**H.T No**

**Regulations:**

**A15**



**Sreenidhi Institute of Science and Technology**

(An Autonomous Institution)

**Code No: 5C629 Date: 07-June-2019 (FN)**

**B.Tech III-Year II-Semester External Examination, May/June-2019 (Supplementary)**

**STRUCTURED DIGITAL SYSTEM DESIGN (ECE)**

**Time: 3 Hours Max.Marks:75**

***Note: a****) No additional answer sheets will be provided.*

*b) All sub-parts of a question must be answered at one place only, otherwise it will not be valued.*

*c) Missing data can be assumed suitably.*

**Part - A Max.Marks:25**

**Answer all QUESTIONS.**

|  |  |  |
| --- | --- | --- |
| 1. | Define fan-out and fan-in. | [3M] |
| 2. | What is mean by clock skew? | [3M] |
| 3. | Discuss the steps involved in the analysis of sequential circuits. | [3M] |
| 4. | Explain timing considerations in MISC design. | [3M] |
| 5. | Explain the power supply requirements in sequential circuits. | [3M] |
| 6. | List the applications of FPLA’s. | [2M] |
| 7. | Define Noise Margin. | [2M] |
| 8. | Compare Mealy and Moore Machines. | [2M] |
| 9. | Explain about Configurable memories. | [2M] |
| 10. | Analyze the D-Latch Flip-flop. | [2M] |

**Part – B Max.Marks:50**

**ANSWER ANY FIVE QUESTIONS. EACH QUESTION CARRIES 10 MARKS.**

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| 11. | a) | Design a combinational circuit that will compare two bits A and B and produce one of the three out puts?  A > B; A = B; A < B. | [5M] |
|  | b) | Design a BCD adder circuit. | [5M] |
|  |  |  |  |
| 12. | a) | Using timing diagrams of clocked JK flip flop analyze the operation. | [5M] |
|  | b) | Design any two oscillator circuits suitable for digital system clock. | [5M] |
|  |  |  |  |
| 13. | a) | Design a sequence detector which detects 0111 sequence. The circuit samples input on each rising edge of system clock. | [5M] |
|  | b) | Design an odd length (modulo 7) ring counter which is initialized or reset to state 7 (111). | [5M] |
|  |  |  |  |
| 14. | a) | Explain the Multi –Input System Controller design phases. | [5M] |
|  | b) | Draw the flow diagram for a prototype pop vending machine control system. | [5M] |
|  |  |  |  |
| 15. | a) | What is the conditional output? Explain with example. | [5M] |
|  | b) | How to specify the system controller states using MDS diagram? | [5M] |
|  |  |  |  |
| 16. | a) | Explain the first cut flow diagram for a 2’s complement system. | [5M] |
|  | b) | Write about MUX configurable indirect addressed ROMs. | [5M] |
|  |  |  |  |
| 17. | a) | What are the practical aspects of wired logic? | [3M] |
|  | b) | Draw a timing diagram and illustrate SETUP time and HOLDING time. | [4M] |
|  | c) | Write a short note on output decoder. | [3M] |
|  |  |  |  |
| 18. | a) | Explain the process of synchronizing two systems. | [4M] |
|  | b) | What is an equivalent state? | [3M] |
|  | c) | Explain the steps involved in the controller design phase. | [3M] |

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